N- and P-Channel 40-V (D-S) MOSFET

CHARACTERISTICS

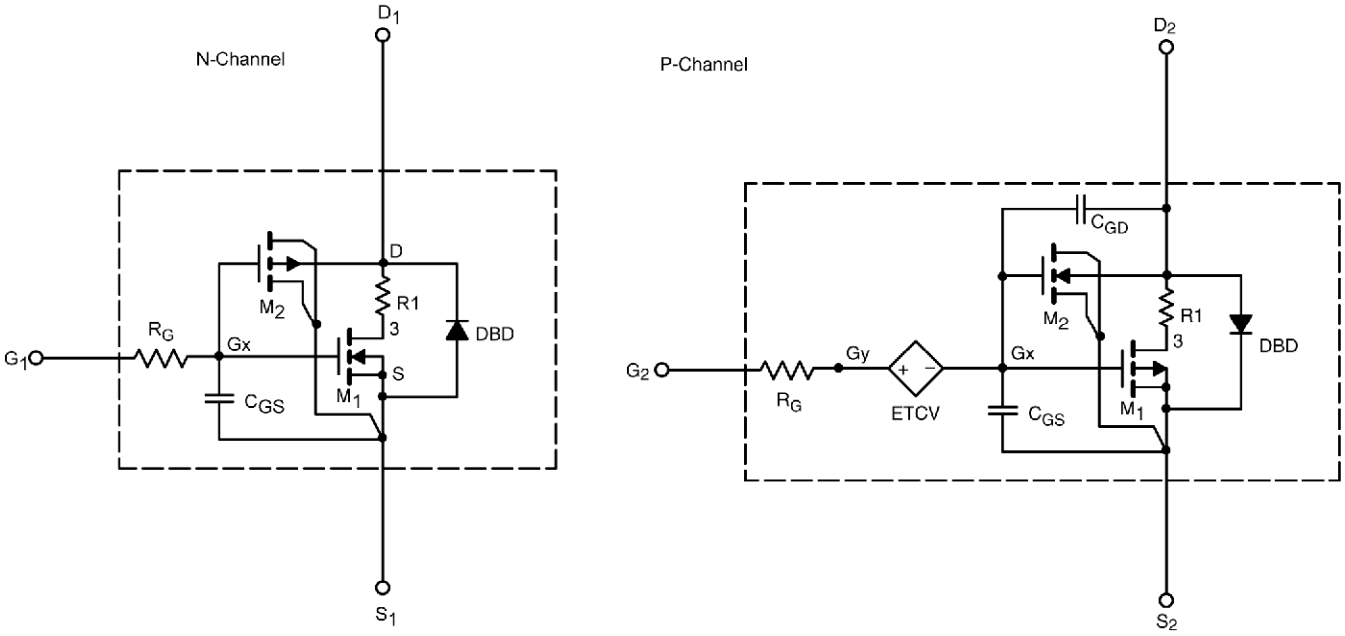
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



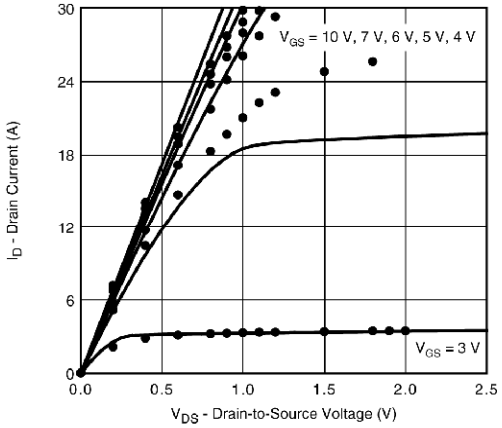
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

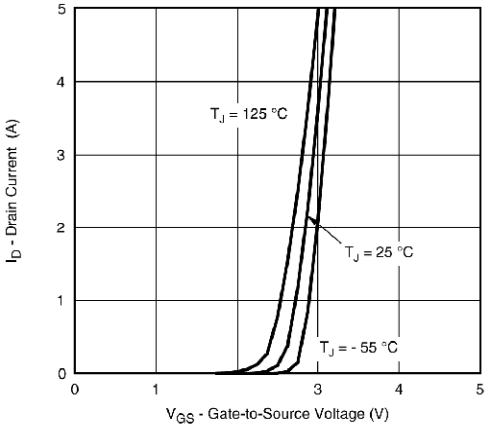
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.8		V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	1.5		
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	N-Ch	0.029	0.0295	Ω
		V_{GS} = - 10 V, I_D = - 5 A	P-Ch	0.038	0.037	
		V_{GS} = 4.5 V, I_D = 4 A	N-Ch	0.0352	0.0355	
		V_{GS} = - 4.5 V, I_D = - 4 A	P-Ch	0.051	0.050	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 5 A	N-Ch	13	22	S
		V_{DS} = - 15 V, I_D = - 5 A	P-Ch	13	14	
Diode Forward Voltage[a]	V_{SD}	I_S = 2 A, V_{GS} = 0 V	N-Ch	0.71	0.78	V
		I_S = - 2 A, V_{GS} = 0 V	P-Ch	0.76	- 0.76	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 20 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	641	640	pF
			P-Ch	965	970	
Output Capacitance	C_{oss}		N-Ch	72	73	
			P-Ch	114	120	
Reverse Transfer Capacitance	C_{rss}		N-Ch	34	41	
			P-Ch	92	95	
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 5 A	N-Ch	10	11.7	nC
		V_{DS} = - 20 V, V_{GS} = –10 V, I_D = - 5 A	P-Ch	19	25	
		N-Channel V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 5 A P-Channel V_{DS} = - 20 V, V_{GS} = - 4.5 V, I_D = - 5 A	N-Ch	5.1	5.3	
			P-Ch	10	11.8	
Gate-Source Charge	Q_{gs}		N-Ch	1.9	1.9	
			P-Ch	3	3	
Gate-Source Charge	Q_{gs}		N-Ch	1.7	1.7	
			P-Ch	5.2	5.2	

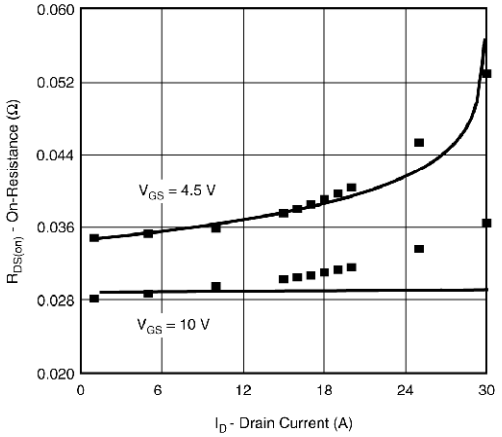
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

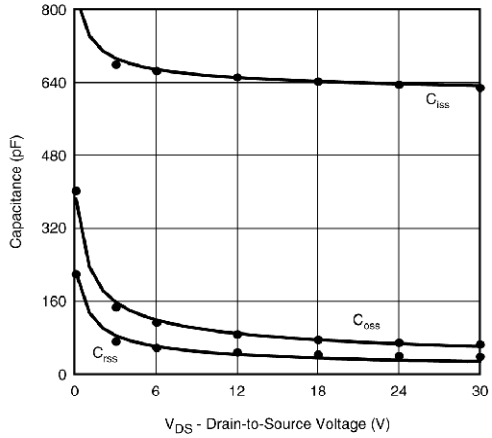
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C UNLESS OTHERWISE NOTED)

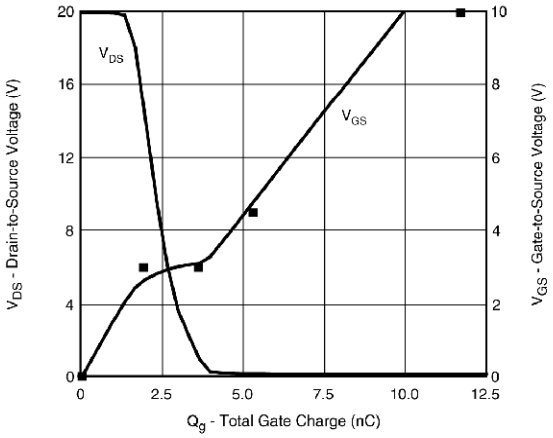
N-Channel MOSFET

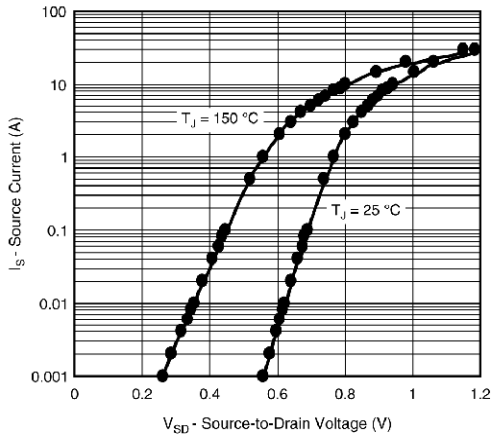








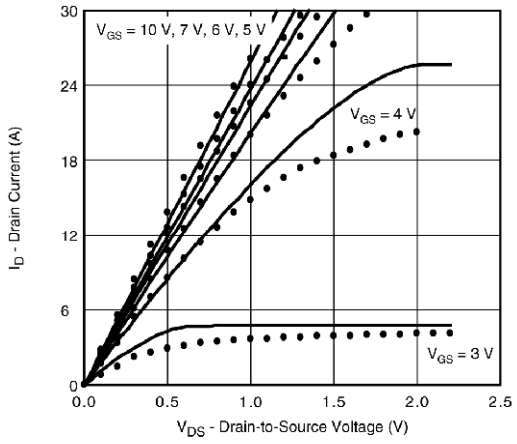


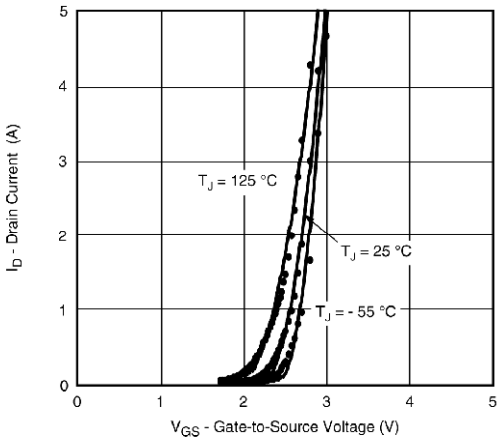


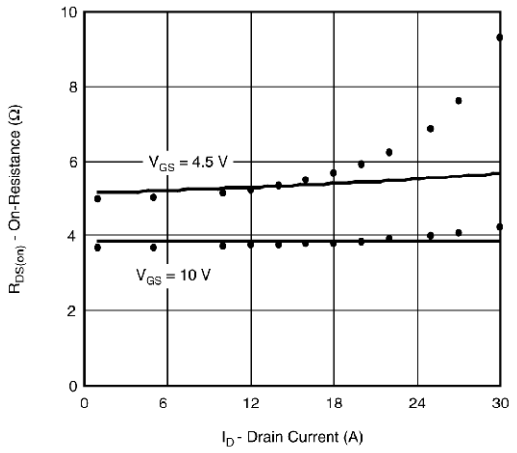
Note: Dots and squares represent measured data.

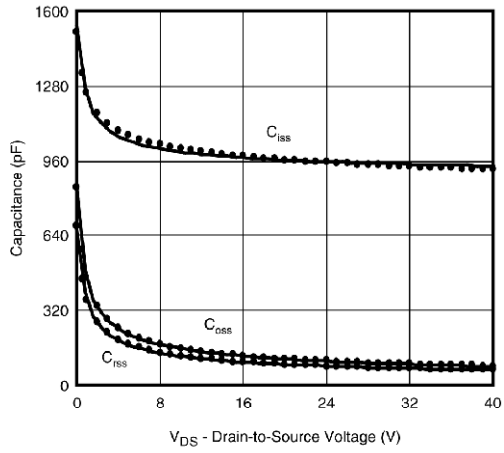
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C UNLESS OTHERWISE NOTED)

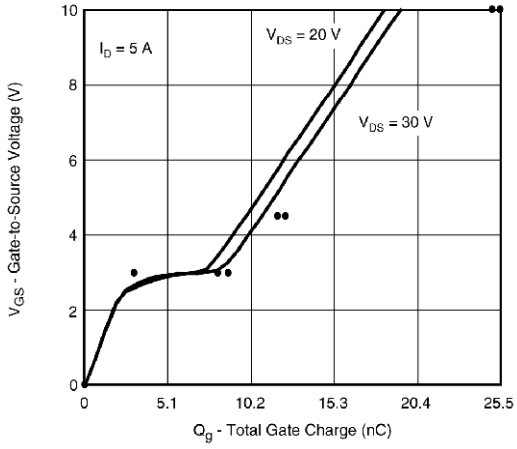
P-Channel MOSFET

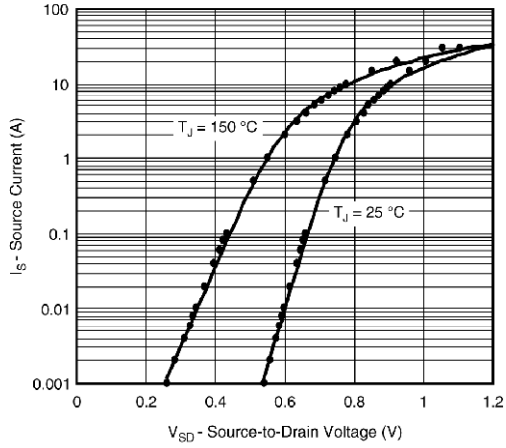












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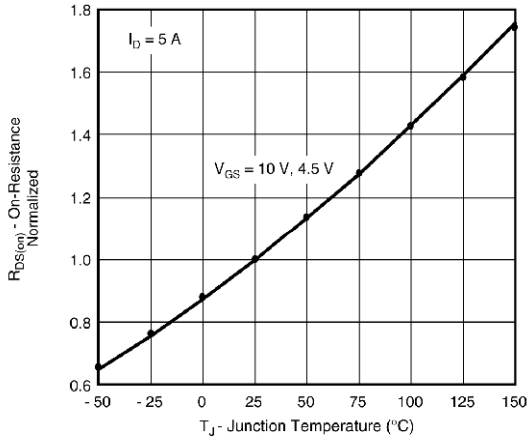
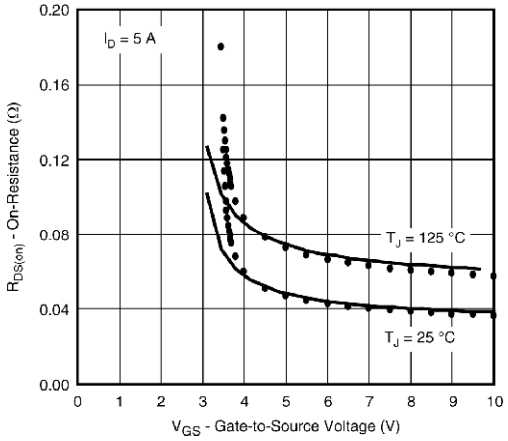
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C UNLESS OTHERWISE NOTED)

P-Channel MOSFET





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